



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,354	06/21/2001	Keiji Yoshizawa	152-01	4463

7590 11/05/2004

Paul & Paul
2900 Two Thousand Market Street
Philadelphia, PA 19103

EXAMINER

SHARON, AYAL I

ART UNIT	PAPER NUMBER
----------	--------------

2123

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/886,354

Applicant(s)

YOSHIZAWA, KEIJI

Examiner

Ayal I Sharon

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 June 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-6 and 10-12 is/are allowed.
- 6) ☒ Claim(s) 1-3 and 7-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 9/27/2001.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-12 of U.S. Application 09/886,354 filed on 06/21/2001 are presented for examination. The application claims priority to Japanese application 2000-188197, filed on 6/22/2000.

Claim Rejections - 35 USC § 101

2. Claim 1-3 and 7-9 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims are directed to solely an abstract idea or to manipulation of abstract ideas, and do not produce a useful result. The claims are devoid of any limitation to a practical application in the technological arts. See MPEP §2106 (II)(A), and *Musgrave*, 431 F.2d at 893, 167 USPQ at 289; *In re Foster*, 438 F.2d 1011, 1013, 169 USPQ 99, 101 (CCPA 1971). The claims have been given the broadest reasonable interpretation, which is that of manually implemented mathematical algorithms.

To be statutory, the utility of an invention must be within the technological arts. *In re Musgrave*, 167 USPQ 280, 289-90 (CCPA, 1970). The definition of "technology" is the "application of science and engineering to the development of machines and procedures in order to enhance or improve human conditions, or

at least to improve human efficiency in some respect.” (Computer Dictionary 384 (Microsoft Press, 2d ed. 1994)).

The limitations recited in claims 1 and 7 contain no language suggesting that claim 1 is intended to be within the technological arts; please note that the method steps of claim 1 and 7, when recited as part of a “computer-implemented method” as in claims 4 and 10, are considered as directed to the technological arts.

Allowable Subject Matter

3. Claims 4-6 and 10-12 are allowed.

4. The prior art used in the Examiner’s reasons for allowance is as follows:
5. Ichiro et al., Japanese Patent Abstract Publication No. 05-334395. (Henceforth referred to as “**Ichiro**”).
6. Liebmann et al., U.S. Patent 5,740,068. (Henceforth referred to as “**Liebmann**”).
7. In regards to Claim 4, Ichiro teaches the following limitations:
 4. A computer readable storage medium having a reduction processing program stored thereon for causing a computer to execute program steps comprising:
 - an offset figure generating step for generating, based on a geometric figure having a plurality of vertices, an offset figure by translating sides, formed by joining said vertices, inwardly of said geometric figure by a distance equal to a prescribed sizing amount;(Ichiro, especially Drawings 2A and 2B, as well as paragraphs [0011] to [0022] in the translated specification.)

While Ichiro does not teach the following limitations, Liebmann does teach them:

Art Unit: 2123

an offset locus line segment generating step for generating an offset locus line segment by joining each of said vertices to an offset vertex corresponding to said each vertex, said offset vertex being located on said offset figure;
(Liebmann, especially: Fig.9, Item 60 and col.7, line 65 – col.8, line 6)

an intersection point detecting step for detecting a first intersection point at which offset locus line segments associated with an adjacent pair of said vertices intersect each other;
(Liebmann, especially: Fig.9, Item 62 and col.8, lines 6-19)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ichiro with those of Manabe, because doing so "... improves the accuracy of the [OPC] corrections by processing individual feature edges ...". (Liebmann, abstract).

However, neither Ichiro nor Liebmann, either individually, nor in combination, expressly teach the following limitations in combination with the limitations:

an offset vertex deleting step for deleting the offset vertices each located at one end of one of the offset locus line segments intersecting at said first intersection point; and

an offset figure revising step for revising said offset figure by finding a second intersection point at which offset figure line segments, forming said offset figure by joining said offset vertices, intersect each other, and by setting said second intersection point as an offset vertex in place of said deleted offset vertices.

8. Claims 5-6 depend from allowable claim 4, and therefore are also allowable.

9. In regards to Claim 10, Ichiro teaches the following limitations:

10. A computer readable storage medium having a reduction processing method stored thereon for causing a computer to execute program steps wherein reduction processing is applied to a difference figure generated by overlaying two geometric figures, to verify, based on the

Art Unit: 2123

size of said difference figure, the validity of processing applied each of said geometric figures, said program steps comprising:

an offset figure generating step for translating an imaginary straight line from each side of said difference figure inwardly of said figure by a distance equal to a prescribed sizing amount and thereby generating an offset figure bounded by said imaginary straight lines, and for storing a set of offset vertices included in said offset figure as a second vertex set; (Ichiro, especially Drawings 2A and 2B, as well as paragraphs [0011] to [0022] in the translated specification.)

While Ichiro does not teach the following limitations, Liebmann does teach them:

an offset locus line segment generating step for generating an offset locus line segment by joining each vertex of said difference figure to one of said offset vertices that corresponds to said each vertex; (Liebmann, especially: Fig.9, Item 60 and col.7, line 65 – col.8, line 6)

an intersection point detecting step for detecting the presence or absence of a first intersection point at which two offset locus line segments extending from adjacent vertices of said difference figure intersect each other; (Liebmann, especially: Fig.9, Item 62 and col.8, lines 6-19)

a sorting step for sorting said first intersection point in order of increasing distance, based on the distance between said first intersection point and the side of said difference figure which is associated with said two offset locus line segments intersecting at said first intersection point; and (Liebmann, especially: Fig.9, Item 64 and col.8, lines 20-30)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ichiro with those of Manabe, because doing so "... improves the accuracy of the [OPC] corrections by processing individual feature edges ...". (Liebmann, abstract).

However, neither Ichiro nor Liebmann, either individually, nor in combination, expressly teach the following limitations in combination with the limitations:

a vertex revising step for computing a second intersection point which defines an intersection between two offset figure sides that extend from the offset vertices of said two offset locus line segments intersecting at said first intersection point selected by sorting, deleting said offset vertices associated with said selected first intersection point from said second vertex set, storing said second intersection point as a new vertex in said second vertex set, deleting from said first vertex set the vertices of said difference figure that are connected to said two offset locus line segments, and storing said selected first intersection point as a new vertex of said difference figure in said first vertex set .

Also, in regards to the following limitation, Liebmann refers to "edge projections" (e.g., col.5, lines 7-10 and lines 18-22; and Figs.3 and 4), but does not refer to the storage of vertices. Ichiro also does not expressly refer to the storage of vertices.

a first vertex set storing step for storing a set of vertices included in said difference figure as a first vertex set;

10. Claims 11-12 depend from allowable claim 10, and therefore are also allowable.

Conclusion

11. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

12. van den Hove et al. "Optical Lithography Techniques for 0.25um and Below: CD Control Issues." Proc. of Technical Papers, 1995 Int'l Symposium on VLSI

Technology, Systems and Applications. May - June 1995. pp.24-30. This reference teaches correction techniques for optical proximity effects (see pp.25-26). However, these techniques are not taught at the level of detail as described in the claims of this application.

13. Garofalo, J. et al. "Automatic Proximity Correction for 0.35um I-line Photolithography." 1994 NUPAD V. June 1994. pp.92-94. This reference teaches the implications of optical proximity effects, and how they can be corrected (see p.1, para. 2; and Figs.1a and 1b). In addition, it also teaches the "1.5D rules".
14. Baird, M. "EYEESEE: A Machine Vision System for Inspection of Integrated Circuit Chips". Proc. 1985 IEEE Int'l Conf. on Robotics and Automation. Mar. 1995. pp.444-448. This reference teaches the use of "critical dimension measurement" (see p.445) and "registration measurement" (see p.446).
15. Ito, M. "An Automated System for LSI Fine Pattern Inspection Based on Comparison of SEM Images and CAD Data." 1995 IEEE Int'l Conf. on Robotics and Automation. May 1995. col.1, pp.544-549. This reference teaches an automated inspection system based on SEM images and CAD data. Fig.2 (see p.547) shows the algorithm for calculating image positional displacements.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is

Art Unit: 2123

(571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (571) 272-3716.

Any response to this office action should be faxed to (703) 872-9306 or mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

November 1, 2004



KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER